UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/816,955 | 04/05/2004 | Satoshi Otsuka | 042322 | 2296 |

38834 7590 12/15/2005

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

| EXAMINER | |
|---|---|
| GEBREMARIAM, SAMUEL A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/816,955 | OTSUKA, SATOSHI | |
| | Examiner | Art Unit | |
| | Samuel A. Gebremariam | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The substitute specification provided by applicant is acknowledged.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al., US Patent No. 6,680,540 in view of Miyamoto et al. US patent No. 6,670,714.

Regarding claim 1, Nakano teaches (figs. 5, 7a-7h) a semiconductor device comprising: a first inter-layer insulation film (18) formed over a substrate (10a) and including a first low dielectric constant film (18, Silk dielectric) whose dielectric constant is lower than of silicon oxide (layer18 can be Silk dielectric with dielectric constant of 2.65 that is lower than silicon oxide) and a hydrophilic insulation film (19, layer 19 can be formed of silicon oxide which is hydrophilic insulation film, col. 18, lines 30-35) formed on the first low dielectric constant film (18); a first interconnection layer (2) buried in a first inter-layer interconnection trench (7, refer to fig. 7h) formed in the first insulation film (18), whose minimum interconnection pitch is first pitch (interconnection 2 has a certain pitch that is taken as a first pitch); a second inter-layer insulation film (18, the dielectric layer 18 above the first interlayer 18, fig. 5) formed over the first inter-layer

insulation film (18) and including a second low dielectric constant film (18) whose dielectric constant is lower than that of silicon oxide (layer 18 can be Silk dielectric with dielectric constant of 2.65 that is lower than silicon oxide); a second interconnection layer (the interconnection layer 2 in the middle part of fig. 5) buried in a second interconnection trench formed (7, fig. 7h) in the second inter-layer insulation film (18) whose minimum pitch is a second pitch (the middle interconnection has a certain pitch that is a second pitch), a diffusion preventing film (barrier film 3) formed directly on the second low dielectric constant film and (layer 3 is formed directly on the side surface of the second low dielectric constant film 18 and the second interconnection layer 2, refer to the middle part of fig. 5) the second interconnection layer.

Nakano does not explicitly state that the second pitch is larger than the first pitch.

Miyamoto teaches (fig. 4) a multi-level interconnection structure whose minimum interconnection pitch is a first pitch (interconnections formed in the lower part of fig. 4) and a second interconnection pitch is a second pitch larger (interconnections formed in the middle region have a second pitch that is larger than the lower region) than the first pitch in order to prevent contact failure from occurring and improve the reliability of the semiconductor device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of multi-level interconnection with different pitches in the structure of Nakano in order to prevent contact failure from occurring and improve the reliability of the semiconductor device.

Regarding claim 2, Nakano teaches substantially the entire claimed structure of claim 1 above including a third inter-layer insulation film (the interlayer insulating layer 18, formed on the top portion of the interconnection structure) formed over the second inter-layer insulation film (inter layer 18 in the middle) and including an insulation film (18, note that the insulating film can be made of inorganic insulation film such as silicon oxide and has a dielectric constant higher than the first and second low dielectric constant films) having dielectric constant higher than the first low dielectric constant film and the second low dielectric constant film and third interconnection layer (the interconnection layer on the top portion of the interconnect structure 2) buried in a third trench formed in the third inter-layer insulation film (refer to fig. 7h), whose minimum interconnection pitch is a third pitch.

Nakano does not explicitly teach the third pitch is larger than the first pitch and second pitch.

Miyamoto teaches (fig. 4) a multi-level interconnection structure whose minimum interconnection pitch is a first pitch (interconnections formed in the lower part of fig. 4), a second interconnection pitch is a second pitch larger (interconnections formed in the middle region have a second pitch that is larger than the lower region) than the first pitch and a third pitch (interconnection formed on the upper portion of fig. 4) in order to prevent contact failure from occurring and improve the reliability of the semiconductor device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of multi-level interconnection with

different pitches in the structure of Nakano in order to prevent contact failure from occurring and improve the reliability of the semiconductor device.

Regarding claim 3, Nakano teaches substantially the entire claimed structure of claim 1 above including a diffusion preventing film (3) formed directly (on the side surface of the hydrophilic insulation film 19 and the first interconnection layer 2, lower interconnection 2, fig. 5) on the hydrophilic insulation film (19) and the first interconnection layer (2) (refer to fig. 5).

Regarding claim 4, Nakano teaches substantially the entire claimed structure of claim 2 above including a diffusion preventing film (3) formed directly on the hydrophilic insulation film (19) and the first interconnection layer (2) (refer to fig. 5, diffusion prevention film 3 is directly formed on the side surface of the hydrophilic insulation film 19 and on the side surface of the lower interconnection layer 2).

Regarding claim 5, Nakano teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the second pitch is 1.5 or more times the first pitch.

Parameters such as pitch and width in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the first and second pitch in the structure of Nakano as claimed in order to prevent contact failure from occurring and improve the reliability of the semiconductor device.

Regarding claim 6, Nakano teaches substantially the entire claimed structure of claim 2 above except explicitly stating that the second pitch is 1.5 or more times the first pitch.

Parameters such as pitch and width in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the first and second pitch as claimed in the structure of Nakano in order to prevent contact failure from occurring and improve the reliability of the semiconductor device.

Regarding claim 7, Nakano teaches substantially the entire claimed structure of claim 1 above including the low dielectric constant film is a SiLK film (col. 18, lines 18-30).

Regarding claim 8, Nakano teaches substantially the entire claimed structure of claim 1 above including the interconnection layer (2) is buried in a via hole (fig. 5) formed the inter-layer insulation film (18) and in the interconnection trench formed in a region of the inter-layer insulation film, which includes the via hole (refer to figs. 5 and 7h).

Regarding claim 9, Nakano teaches substantially the entire claimed structure of claim 1 above including the main material of the interconnection layer is Cu (col. 18, lines 5-12).

Regarding claim 10, Nakano teaches (figs. 5 and 7a-7h) a semiconductor device comprising: a first interconnection layer (2, bottom portion of fig. 5) formed over substrate (10a, fig. 7a) and including plurality interconnection layers (fig. 5) whose minimum interconnection pitch is first pitch (fig. 5), at least one of the interconnection layers being buried in an opening formed in a first inter-layer insulation film (18, refer to fig. 7h) including a first low dielectric film (18 is formed of Silk and has a dielectric constant lower than silicon oxide) whose dielectric constant is lower than that of silicon oxide and a hydrophilic insulation film (19, is formed of silicon oxide therefore hydrophilic) formed on the first low dielectric constant film (18); and a second interconnection layer (middle interconnection 2) formed over the first interconnection layer (2) and including minimum interconnection layers whose interconnection pitch is a second pitch, the plurality of the interconnection layers being buried in openings formed in a plurality of second interlayer insulation film (18 and refer to fig. 7h, where the process is shown for forming the first interconnection, but the process is repeated to form the structure in fig. 5) including a diffusion prevention film (3, barrier layer) and a second low dielectric constant film (layer 18 formed in the middle) whose dielectric constant is lower than that of silicon oxide (18 is formed of Silk and has a dielectric constant lower than silicon oxide), the second low dielectric constant film (the middle 18 is formed on the diffusion preventing film 3 of the first interconnection layer), the respective openings being formed in the respective second inter-layer insulation film (18, middle), the respective interconnection layers (2, middle) being buried in the respective openings (refer to figs. 7a-7h).

Nakano does not explicitly teach a first multilayer interconnection layer, a second multilayer interconnection layer formed over the first multilayer interconnection layer whose minimum interconnection pitch is larger than the first pitch or the diffusion preventing film of one second inter-layer insulation film being formed directly on the second low dielectric constant film of another second inter-layer insulation film underlying said one second inter-layer insulation film.

Miyamoto teaches (fig. 4) a first multilayer interconnection layer (bottom interconnection, fig. 4) including plurality of interconnections layers whose minimum interconnection pitch is a first pitch (fig. 4) and a second multilayer interconnection layer (middle interconnection) formed over the first multilayer interconnection layer whose minimum interconnection pitch is larger than the first pitch (bottom interconnection has smaller pitch than the middle interconnection layers, fig. 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the first and second multilayer interconnection layers with different pitch taught by Miyamoto in the structure of Nakano in order in order to form a multilayer interconnection structure with improved reliability.

Furthermore the combined structure of Nakano and Miyamoto teaches the diffusion preventing film of one second inter-layer insulation film being formed directly on the side surfaces of the second low dielectric constant film of another second inter-layer insulation film underlying the one second inter-layer insulation film.

Regarding claim 11, Nakano teaches substantially the entire claimed structure of claim 10 above except explicitly stating that a third multilayer interconnection layer

formed over the second multilayer interconnection layer and including a plurality of interconnection layers whose minimum interconnection pitch a third pitch larger than the first pitch and the second pitch, the plurality of interconnection layers forming the third multilayer interconnection layer being buried in an opening formed in a third inter-layer insulation film.

However Nakano discloses a third interconnection layer formed over the second interconnection layer where the third interlayer insulation film can be of an inorganic insulation film (col. 18, lines 18-25).

Miyamoto teaches (fig. 4) a third multilayer interconnection layer (the upper interconnection layer of fig. 4) formed over the second multi-level interconnection layer (layer 23 and the layer above it, fig. 4) and including a plurality of interconnection layers whose minimum interconnection pitch is a third pitch (interconnections formed in the upper part of fig. 4) larger than the first pitch and the second pitch (fig. 4) in order to prevent contact failure from occurring and improve the reliability of the semiconductor device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of the multi-level interconnection with different pitches in the structure of Nakano in order to prevent contact failure from occurring and improve the reliability of the semiconductor device. Furthermore it is with the skill one of ordinary skill in the art to pick an inorganic insulating film as the third interlayer insulation film in the structure of Nakano in order to form a reliable interconnection structure that is less prone to failure. Therefore the combined structure

of Nakano and Miyamoto inherently teaches a third interlayer isolation film having dielectric constant higher than the first low dielectric constant film and the second low dielectric constant film.

***Response to Arguments***

4. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
December 2, 2005

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800